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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/683,383	12/20/2001	Jens Leenstra	DE920000098US1	9708

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LAW OFFICE OF IDO TUCHMAN
69-60 108 STREET
SUITE 503
FOREST HILLS, NY 11375

EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/683,383	LEENSTRA ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2004 and 21 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-10 have been considered. Claims 1-10 have been amended as per Applicant's request.

Double Patenting

2. Applicant is advised that should claim 6 be found allowable, claim 10 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k). Claims 6 and 10 have the exact same limitations and their differences are only found in the preamble of the claims. Claim 10's "a computer system having an out-of-order processing system" is encompassed in scope of claim 6's "a processing system having means for executing", since "a processing system" encompasses "a computer system having an out-of-order processing system" in its scope. Also, the preamble of a claim is not generally given patentable weight.

Papers Submitted

3. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 24 November 2004; Change of Address as received on 24 January 2005; and Amendment as received on 21 March 2005.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-6 and 10 are rejected under 35 U.S.C. 102(b) as being taught by Gaertner et al., U.S. Patent Number 5,996,063 (herein referred to as Gaertner).

6. Referring to claim 1, Gaertner has taught a method for operating an out-of-order processor comprised of an instruction pipeline, the method comprising the steps of:

a. For detection of a dependency, determining for each current instruction involved in a renaming process that a logic target address of one or more instructions is not the same as a logic source address of said current instruction said one or more instructions being stored in a temporary buffer associated with a pipeline process downstream of the current instruction (Gaertner column 8, lines 6-54; Figure 2; Figure 3; and Figure 4);

b. Generating a no-dependency signal associated with said current instruction (Gaertner column 8, lines 6-54; Figure 2; Figure 3; and Figure 4). In regards to Gaertner, the system detects when there is a dependency or not and acts upon this signal, i.e. the signal shows whether there is a dependency or no dependency.

c. If the no-dependency signal is not active assigning an entry in the temporary buffer to the logic source address of said current instruction (Gaertner column 8, lines 6-54; Figure 2; Figure 3; and Figure 4); and

d. if the no-dependency signal is active issuing the instruction operand data to an instruction execution unit without assigning the entry in the temporary buffer to the logic source address of said current instruction (Gaertner column 8, lines 6-54; Figure 2; Figure 3; and Figure 4).

7. Referring to claim 2, Gaertner has taught

a. Comparing a plurality of logic target register addresses and the logic source register address of the current instruction in case the no-dependency signal is not active (Gaertner column 8, lines 6-54; Figure 2; Figure 3; and Figure 4); and

b. Generating a dependency signal for the respective source register (Gaertner column 8, lines 6-54; Figure 2; Figure 3; and Figure 4). In regards to Gaertner, the signal is inherent since the signal is needed in order for the appropriate actions with the reorder buffer and rename units to be done.

8. Referring to claim 3, Gaertner has taught evaluating 'valid'-bits of speculative target registers stored in a storage associated with speculatively calculated instruction result data to generate the no-dependency signal (Gaertner column 8, lines 6-54; Figure 2; Figure 3; and Figure 4).

9. Referring to claims 4 and 5, Gaertner has taught

a. Addressing a mapping-table-entry with a logical source register address of said current instruction thus determining the mapped physical target register address (Gaertner column 8, lines 6-54; Figure 2; Figure 3; and Figure 4);

b. Reading a committed-status flag in said entry (Gaertner column 9, line 66 to column 10, line 32 and Figure 4);

c. Comparing the logic target register address and the logic source register address of the current instruction in case the no-dependency signal is not active (Gaertner column 8, lines 6-54; column 9, line 66 to column 10, line 32; Figure 2; Figure 3; and Figure 4); and

d. Generating a dependency signal for the respective source register (Gaertner column 9, line 66 to column 10, line 32 and Figure 4).

10. Referring to claims 6 and 10, Gaertner has taught a processing system having means for executing a readable machine language (Applicant's claim 6), and a computer system having an out-of-order processing system, said computer system executes a readable machine language (Applicant's claim 10), said readable machine language comprises:

a. A first computer readable code for, the detection of a dependency, determining for each current instruction involved in a renaming process that a logic target address of one or more instructions stored in a temporary buffer associated with a pipeline process downstream of the current instruction is not the same as a logic source address of said current instruction (Gaertner column 8, lines 6-54; Figure 2; Figure 3; and Figure 4),

b. A second computer readable code for generating a no-dependency signal associated with said current instruction (Gaertner column 8, lines 6-54; Figure 2; Figure 3; and Figure 4),

c. A third computer readable code for assigning an entry in the temporary buffer to the logic source address of said current instruction if the no-dependency signal is not active (Gaertner column 8, lines 6-54; Figure 2; Figure 3; and Figure 4), and

d. A fourth computer readable code for issuing the instruction operand data to an instruction execution unit without assigning the entry in the temporary buffer to the logic source address of said current instruction if the no-dependency signal is active (Gaertner column 8, lines 6-54; Figure 2; Figure 3; and Figure 4).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaertner et al., U.S. Patent Number 5,996,063 (herein referred to as Gaertner) in view of Garg et al., U.S. Patent No. 5,974,526 (herein referred to as Garg). Gaertner has not taught

a. In case of a content-addressable memory (CAM)-based renaming scheme the first computer readable code for determining the dependency of a current instruction comprises a compare logic in which all instructions to be checked for dependency are involved and an OR gate coupled with the compare logic (Applicant's claims 7 and 9).

b. A plurality of AND gates the input of which comprises a target register 'valid bits' signal and a respective compare logic output signal (Applicant's claim 8).

13. However, Gaertner has taught that there is some type of look-up is performed (Gaertner column 8, lines 6-54; column 9, line 66 to column 10, line 32; Figure 2; Figure 3; and Figure 4), but not the exact gate structure. Garg has taught a look-up table

a. In case of a content-addressable memory (CAM)-based renaming scheme (see Garg, Col.8 lines 38-65 and Col. 12 lines 42-58) the first computer readable code for determining the dependency of a current instruction comprises a compare

logic in which all instructions to be checked for dependency are involved and a post-connected OR gate (see Garg, 206 of Fig.2 and 700 of Fig.7). Here, each generic comparison block (see Garg, 204 of Fig.2) performs three separate comparisons on a current and prior instructions operands (see Garg, Fig.7), and the generic comparison block outputs that a dependency exists if any of the three individual comparisons are true (see Garg, Col. 10 line 56 - Col. 11 line 46). Further, the mapping-table based renaming system used by Garg (see Garg, Col.8 lines 38-65 and Col. 12 lines 42-58) is also inherently content-addressable, as it is indexed into using contents of its registers (see Garg, Col. 12 lines 42-58).

b. A plurality of AND gates (see Garg, 808 of Fig.8) the input of which comprises the target register ("valid-bits" signal (see Garg, 512/514 of Fig.5 and Col. 10 lines 56-61) and a respective compare logic output signal (see Garg, Figs. 2, 7 and 8). Here, there is a plurality of AND gates (see Garg, 808 of Fig.8) because the circuit of Fig.8 is duplicated three times in comparators 702, 704 and 706, as well as many times in the Data Dependency Checker (see Garg, Fig.2 and Col. 10 line 56 - Col. 11 line 46).

14. A person of ordinary skill in the art at the time the invention was made would have recognized that Garg's table allows for tracking of values to the renamed registers (Garg column 4, lines 33-40), thereby ensuring that the values are correctly mapped and can be written to the physical registers correctly. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the table of Garg in the device of

Gaertner to ensure correct mapping of values to renamed registers and correct data being written into the physical registers.

Response to Arguments

15. Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Gaertner et al., U.S. Patent Number 6,108,771, has taught register renaming.

17. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

18. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

20. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

21. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
31 May 2005

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
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